TRANSMITTAL LETTER Docket No. (General - Patent-Issued) BUR920040170US1 Patentee(s): Anderson et al. APR 2 8 2006 U.S. Patent No. **Issue Date** 7,012,316 03-14-2006 Title: ISOLATION STRUCTURES IN SEMICONDUCTOR INTEGRATED CIRCUITS **COMMISSIONER FOR PATENTS:** Transmitted herewith is: Certificate **Certificate of Correction** MAY 0 3 2006 Post card of Correction No fee required below. Errors were made by the United States Patent Office. No additional fee is required. A check in the amount of is attached. The Director is hereby authorized to charge and credit Deposit Account No. 09-0456 (IBM) as described below. Charge the amount of X Credit any overpayment.  $\boxtimes$ Charge any additional fee required. Jan P. Fredner Dated: 04-19-2006 Jack P. Friedman, Ph.D. Reg. No. 44,688 I certify that this document and fee is being deposited Schmeiser, Olsen & Watts on 04-19-2006 with the U.S. Postal Service as 22 Century Hill Drive, Suite 302 first class mail under 37 C.F.R. 1.8 and is addressed to the **Latham, NY 12110** Commissioner for Patents, P.O. Box 1450, Alexandria, VA (518) 220-1850 22313-1450. Customer No.: 30449 Signature of Person Mailing Correspondence

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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 7,012,316

DATED : March 14, 2006

INVENTOR(S): Anderson et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4

Line 50, delete "stop" and insert -- step --

Column 5

Line 18 and line 21, delete "or" and insert -- of --

Column 6

Line 2, delete "cup" and insert -- cap --

MAILING ADDRESS OF SENDER: Jack P. Friedman, Ph.D.

Reg. No. 44,688 Schmeiser, Olsen & Watts 22 Century Hill Drive, Suite 302 Latham, NY 12110 PATENT NO. 7,012,316

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